EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("20030088826").PN.	US-PGPUB; USPAT	OR	OFF	2007/06/11 06:59
L2	789	(710/316).ccls.	US-PGPUB; USPAT	OR	OFF	2007/06/11 07:15
L3	315	(710/317).ccls.	US-PGPUB; USPAT	OR	OFF	2007/06/11 07:37
L4	405	(712/220).ccls.	US-PGPUB; USPAT	OR	OFF	2007/06/11 08:21
L5	3071	(709/238).ccls.	US-PGPUB; USPAT	OR	OFF	2007/06/11 07:01
L6	0	(715/201.1).ccls.	US-PGPUB; USPAT	OR	OFF	2007/06/11 07:01
L7	1540	(715/501.1).ccls.	US-PGPUB; USPAT	OR	OFF	2007/06/11 07:02
L8	2	("5771362" "7028134").pn.	US-PGPUB; USPAT	OR	OFF	2007/06/11 09:02
L9	4	("6142683" "5561761" "5941968" "5610981").PN.	US-PGPUB; USPAT	OR	OFF	2007/06/11 09:09
L10	780	"DATA STEERING"	US-PGPUB; USPAT	OR	OFF	2007/06/11 09:09
L11	499	L10 AND @AD<"20011106"	US-PGPUB; USPAT	OR	OFF	2007/06/11 09:16
L12	15	L11 AND "FUNCTIONAL UNIT"	US-PGPUB; USPAT	OR	OFF	2007/06/11 09:15
L13	43	STEER$3 WITH "CONTROL WORD"	US-PGPUB; USPAT	OR	OFF	2007/06/11 09:15
L14	20	L13 AND @AD<"20011106"	US-PGPUB; USPAT	OR	OFF	2007/06/11 10:35
L15	49	("4764925" "4903150" "5361363" "5872987" "6141313" "6219775" "6219775" "4357658" "4443850" "5333268" "5353412" "5388214" "5390298" "5513366" "5530809" "5537535" "5590283" "5680550" "5758176" "5805920" "5825749" "6239628" "4437711" "4527285" "4763304" "4780599" "4811214" "4866604" "4878203" "4922413" "5195052" "5204866" "5265207" "5398331" "5423051" "5452466" "5475860" "5481743" "5557545" "5564056" "5574928" "5574942" "5583754" "5612640" "5615385" "5623685" "5712972" "5778247" "5778210" "5793946").pn.	US-PGPUB; USPAT	OR	OFF	2007/06/11 10:35

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J Hauser
K Mai
P Guerrier
R Hartenstein

[BOOK] Smart Memories: A Modular Reconfigurable Architecture - all 17 versions »
K Mai, T Paaske, N Jayasena, R Ho, WJ Dally, ... - 2000 - Defense Technical Information Center
... buses may also be configured as half- **word** buses. ... to these buses, a small number of **control** bits are ... on each tile connects the internal tile **crossbar** to the ...
Cited by 179 - Related Articles - Web Search - Library Search - BL Direct

The NAPA adaptive processing architecture - all 7 versions »
CR Rupp, M Landguth, T Garverick, E Gomersall, H ... - FPGAs for Custom Computing Machines, 1998. Proceedings. IEEE ..., 1998 - ieeexplore.ieee.org
... Although not as flexible as a **crossbar** style interconnect structure, the ToggleBus nevertheless implements all of the major ... Pipeline **Control** Ports ... Status **Word** ...
Cited by 115 - Related Articles - Web Search

A low-power, high-performance, 1024-point FFT processor - all 6 versions »
BM Baas - Solid-State Circuits, IEEE Journal of, 1999 - ieeexplore.ieee.org
... and from (1), the cache size equals **words**. ... the chip also contains **crossbar**, **control**, clock generation ... a brief overview of each **functional unit** type, followed by ...
Cited by 72 - Related Articles - Web Search - BL Direct

Multiprocessor coupling system with integrated compile and run time scheduling for parallelism - all 4 versions »
SW Keckler, WJ Dally - US Patent 5,574,939, 1996 - Google Patents
... Timeout Limit Register, and a **control word** containing HALT ... Finally, the Global **Control**
Unit sequen- tializes the ... C-Switch) 24 is a **crossbar** switch withfourbuses ...
Cited by 67 - Related Articles - Web Search

Wormhole run-time reconfiguration - all 14 versions »
R Bittner, P Athanas - Proceedings of the 1997 ACM fifth international symposium on ..., 1997 - portal.acm.org
... used to inject the exponent and mantissa **words** of the ... the new input to gain exclusive **control** of the ... small and reside compactly underneath the **crossbar** routing ...
Cited by 45 - Related Articles - Web Search

Architecture design of reconfigurable pipelined datapaths - all 8 versions »
DC Cronquist, C Fisher, M Figueroa, P Franklin, C ... - Advanced Research in VLSI, 1999. Proceedings. 20th ..., 1999 - ieeexplore.ieee.org
... Unfortunately, the chip area of the **crossbar** scales with ... The buses are **word**-based instead of bit based ... simplies the layout and reduces the **control** requirements ...
Cited by 81 - Related Articles - Web Search

A generic architecture for on-chip packet-switched interconnections - all 22 versions »
P Guerrier, A Greiner - Proceedings of the conference on Design, automation and test ..., 2000 - portal.acm.org

... The regular parts (buffers and **crossbar**) were placed manually ... Figure 7: Router floorplan
The **control** logic can ... network (16 routers) with 20-**word** packets spread ...
Cited by 289 - Related Articles - Web Search

Garp: A MIPS Processor with a Reconfigurable Coprocessor - all 24 versions »
JR Hauser, J Wawrzynek - IEEE Symposium on FPGAs for Custom Computing Machines, 1997 - doi.ieeecs.org
... row serve as liaisons between the array and the outside world. Among other things, **control** blocks can interrupt the main ... **crossbar crossbar crossbar crossbar** ...
Cited by 498 - Related Articles - Web Search

Colt: An Experiment in Wormhole Run-time Reconfiguration - all 12 versions »
R Bittner, P Athanas, M Musgrove - SPIE Photonics East96, Boston, MA, USA, Nov, 1996 - 128.173.52.3
... receive their northern local inputs and skip bus connections from the **crossbar**. ... Outputs To **Cross Bar** ... It consists of the FU surrounded by the **control** and buses ...
Cited by 24 - Related Articles - View as HTML - Web Search

Logical, fail-**functional**, dual central processor units formed from three processor units - all 3 versions »
RW Horst - US Patent 5,838,894, 1998 - Google Patents
... The system achieves a low cost fail-**functional** architecture. 7Claims, 30 Drawing Sheets Page 2. ... FIG. 16. INTERNAL **CONTROL** ERROR ERROR ... I EVEN **WORDS** ODD **WORDS** 28 ...
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W Coates
J Fridman
C Wakeland
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FLEETzero: An Asynchronous Switching Experiment - all 14 versions »
WS Coates, JK Lexau, IW Jones, SM Fairbanks, IE ... - Proc. of the Seventh International Symposium on Advanced ..., 2001 - doi.ieeecomputersociety.org
... for example, point-to-point, **crossbar**, or butterfly ... our chip interfaces to make **functional** testing possible ... includes adjustable delays in most **control** modules. ...
Cited by 21 - Related Articles - Web Search

The TigerSHARC DSP architecture - all 9 versions »
J Fridman, Z Greenfield, AD Inc, MA Norwood - Micro, IEEE, 2000 - ieeexplore.ieee.org
... Each data bus has associated 32-bit address and **control** buses ... to the compiler comes from the very long instruction **word** (VLIW) approach ... Memory interface **crossbar** ...
Cited by 67 - Related Articles - Web Search - BL Direct

System and method of routing communications data with multiple protocols using **crossbar** switches - all 3 versions »
C Wakeland... - US Patent 5,905,873, 1999 - Google Patents
... DATA WITH MULTIPLE PROTOCOLS USING **CROSSBAR** SWITCHES ... preferably includes arbitration
and **control** logic for ... embodiment, the single-sided **cross-bar** switch is ...
Cited by 30 - Related Articles - Web Search

Communication traffic circle system and method for performing packet conversion and routing between ... - all 3 versions »
AC Hartmann, CK Wakeland... - US Patent 6,047,002, 2000 - Google Patents
... preferably includes arbitration and **control** logic for ... embodiment, the single-sided **cross-bar** switch is ... architec- ture and/or **crossbar** switch architecture for ...
Cited by 27 - Related Articles - Web Search

Apparatus for coupling a bus-based architecture to a switch network - all 2 versions »
HT Olnowich, MW Dotson, JW Feeney, MH Fisher, JD ... - US Patent 6,263,374, 2001 - Google Patents
... 2SWITCH ADAPTER (SA) -MC ADDRESS - LINES -MC **CONTROL** — SIGNALS —MC DATA LINES r ... 4X4
ALLNODE SWITCH ALLNODE &CONNECTION **CONTROL** 1 cr\ A «• 1RF.I -IN1-ACC ...
Cited by 7 - Related Articles - Web Search

An industrial view of electronic design automation - all 6 versions »
D MacMillen, R Camposano, D Hill, TW Williams - Computer-Aided Design of Integrated Circuits and Systems, ..., 2000 - ieeexplore.ieee.org
... starting "temperatures" sometimes in the **units** of "million ... escaping from SPICE for **functional** verifica- tion. ... in the larger simulation world outside ECAD ...
Cited by 19 - Related Articles - Web Search - BL Direct

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All Results
C Wakeland
J Palys
G Busenberg
D Wiley
V Zyuban

Debug interface including **data steering** between a processor, an input/output port, and a trace logic - all 2 versions »
US Patent 6,142,683, 2000 - freepatentsonline.com
A system for debugging a processor includes a **data steering** circuit for steering commands and data from a debug port and a parallel input/output port. ...
Cited by 19 - Related Articles - Cached - Web Search

Central processing unit data entering and interrogating device and method therefor - all 3 versions »
GD Hicok, JA Lehman, T Alexander, YJ Lim, DR Evoy, ... - US Patent 5,561,761, 1996 - Google Patents
... r\WU K 1—wO Ì-.M » ^ti i DEVICEsen i- **DATA STEERING**? \ \ ^ ... The selection portion46 has adevice select line 50 connected to the **data steering** portion 52. ...
Cited by 35 - Related Articles - Web Search

Computer system for concurrent data transferring between graphic controller and unified system ... - all 3 versions »
JO Mergard, MS Quimby, CK Wakeland... - US Patent 5,941,968, 1999 - Google Patents
... [57] ABSTRACT Acomputer system is provided including a CPU, a graphics controller, system memory, **data steering** logic, a DMA controller and arbitration logic. ...
Cited by 26 - Related Articles - Web Search

The IPCS Collaborative Study on Neurobehavioral Screening Methods: IV. Control **data**. **Steering** Group. - all 3 versions »
VC Moser, GC Becking, V Cuomo, E Frantik, BM Kulig ... - Neurotoxicology, 1997 - ncbi.nlm.nih.gov
The IPCS Collaborative Study on Neurobehavioral Screening Methods: IV. Control **data**. **Steering** Group. Moser VC, Becking GC, Cuomo ...
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A 500 MHz 1.5 MB cache with on-chip CPU
J Lachman, JM Hill - Solid-State Circuits Conference, 1999. Digest of Technical ..., 1999 - ieeexplore.ieee.org
... reset and data is transferred to registers driving the adjustable delay circuit shown in Figure 11.2.3. Yield is enhanced by a **data steering** column redundancy ...
Cited by 8 - Related Articles - Web Search

Preboot protection for a data security system with anti-intrusion capability - all 3 versions »
DM Mooney, JA Kimlinger, DE Wood... - US Patent 5,610,981, 1997 - Google Patents
... control ASIC 230 is instructed to connect processor 220 to the system bus 292 via **data steering** network 240 and cipher engine 270; enable destruct interrupts ...
Cited by 28 - Related Articles - Web Search

System and method of routing communications data with multiple protocols using crossbar switches - all 3 versions »
C Wakeland... - US Patent 5,905,873, 1999 - Google Patents

Page 1. United States Patent Hartmann et al. US005905873A [il] Patent Number: [45] Date of Patent: [54] SYSTEM AND METHOD OF ROUTING ...
Cited by 30 - Related Articles - Web Search

Collaborative and adversarial analysis in environmental policy - all 3 versions »
GJ Busenberg - Policy Sciences, 1999 - Springer
... **Steering** committee members representing the RCAC and the oil industry then helped the researchers to gather local knowledge on weather, currents, and vessel tra ...
Cited by 43 - Related Articles - Web Search - BL Direct

A low-power reconfigurable data-flow driven DSP system - all 2 versions »
M Wan, H Zhang, M Benes, J Rabaey - Signal Processing Systems, 1999. SiPS 99. 1999 IEEE Workshop ..., 1999 - ieeexplore.ieee.org
... In order to support dedicated links between satellites without reconfiguration overhead and global control, **data steering** elements are embedded in the ...
Cited by 4 - Related Articles - Web Search

System and method for encoding instruction fields within data packets - all 3 versions »
C Wakeland... - US Patent 5,896,383, 1999 - Google Patents
... Serial Comm. Subsystem 250 ». RX FIFO *254 TX FIFO T » 256 k. DRAK Control 232 1er **Data Steering** 242 t' k. L GPIO Logic 262 PCMCI Controll 264 Aer D[1 SD[1 ...
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